WHAT IS CLAIMED IS:

1. A method for fabricating a heterojunction bipolar transistor, comprising the steps of:

laminating a collector layer, a base layer and an emitter layer in this order on a top surface side of a semiconductor substrate;

patterning the collector layer, the base layer and the emitter layer so that an area of an upper layer among the collector layer, the base layer and the emitter layer may become smaller;

forming a surface electrode for ohmic contact on each surface portion of the collector layer, the base layer and the emitter layer;

forming a first via hole which extends through the emitter layer, the base layer and the collector layer and ends at the specified depth within the substrate;

forming a metal wiring line which extends from the surface electrode of the emitter layer to within the first via hole so as to reach a bottom portion of the first via hole;

polishing a rear surface side of the substrate up to the bottom portion of the first via hole; and

providing a heat sink layer made of a metal on the polished rear surface of the substrate so that the heat

sink layer makes contact with the metal wiring line within the first via hole.

2. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

after forming the first via hole, an insulating film is so provided as to cover top surfaces and side surfaces of the emitter layer, the base layer and the collector layer, and the first via hole is furthermore extended toward the rear surface side of the substrate.

3. The method for fabricating a heterojunction bipolar transistor according to claim 2, wherein

a wet etching process or a low-power conditioned dry etching process is performed in the step of forming the first via hole, and

a high-power conditioned dry etching is performed in the step of extending the first via hole toward the rear surface side of the substrate.

4. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

an undercut is formed by etching a lower outer-edge portion of the emitter layer in the process of patterning the emitter layer;

a metal film is deposited on the top surface side of the substrate so as to form the surface electrode of the base layer, with an inner edge of the surface electrode of the base layer formed in self alignment to the emitter layer by using the undercut; and

the metal film and the base layer are continuously etched with the same mask so that an outer edge of the surface electrode of the base layer and an outer edge of the base layer become coincident with each other.

5. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

the first via hole is formed after forming the surface electrodes of the collector layer and the base layer and before forming the surface electrode of the emitter layer;

simultaneously with time when the surface electrode of the emitter layer is formed, a wiring pattern of a same material as that of the surface electrode is formed, the wiring pattern extending from a surface portion of the emitter layer to within the first via hole so as to reach a bottom portion of the first via hole; and

the metal wiring line is formed on the wiring pattern by a plating process.

6. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

after forming the metal wiring line, the rear surface side of the substrate is not polished or the rear surface side of the substrate is polished to a specified extent,

a second via hole is so formed as to extend from the rear surface side of the substrate up to the bottom portion of the first via hole, and

the heat sink layer made of a metal is provided on the rear surface of the substrate so as to make contact with the metal wiring line within the first via hole through the second via hole.

7. The method for fabricating a heterojunction bipolar transistor according to claim 6, wherein

simultaneously with time when the first via hole is formed, an alignment hole deeper than the first via hole is formed from the top surface side of the substrate toward the rear surface side of the substrate in a region other than regions occupied by the emitter layer, the base layer and the collector layer;

the rear surface of the substrate is polished up to a bottom portion of the alignment hole; and

a photolithography process for forming the second via hole is performed with reference to the alignment hole appearing on the rear surface side of the substrate.

8. The method for fabricating a heterojunction bipolar transistor according to claim 6, wherein

the second via hole is formed in conical shape which broadens toward the heat sink layer on the substrate rear surface, and an interior of the second via hole is buried with the same material as that of a heat sink layer.

9. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

the surface electrodes of the collector layer, the base layer and the emitter layer are each formed by a lift-off process into a patterned surface electrode which surround a periphery of a region where the first via hole is to be formed and a portion of which is cut out.

10. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

in the process of polishing the rear surface of the substrate up to the bottom portion of the first via hole, the polishing process is ended, by observing electric resistance of a polishing liquid, at a time point when cut

chips of the metal wiring line within the first via hole mingle into the polishing liquid, causing the electric resistance of the polishing liquid to show a change.

11. The method for fabricating a heterojunction bipolar transistor according to claim 1, wherein

a plurality of sets of the emitter layer, the base layer and the collector layer of the heterojunction bipolar transistor are arrayed on a common semiconductor substrate; and

before the first via hole is formed in each heterojunction bipolar transistor, a device isolation region having a specified thickness is formed between the collector layers of adjacent heterojunction bipolar transistors by performing ion implantation.

12. A high-frequency transmitter or receiver including, as a high-frequency amplifier, the heterojunction bipolar transistor made by the heterojunction bipolar transistor fabricating method as defined in claim 1.